CLAIMS

We claim:

1. A semiconductor device, comprising:

a P-channel MOS field-effect transistor comprising,

a semiconductor substrate;

a gate dielectric on the substrate; and

a calcium and boron doped polysilicon gate electrode on the gate dielectric.

2. The semiconductor device of claim 1 wherein the calcium and boron dopants are present in the polysilicon in a ratio of about 1:4 to 1:1.

3. The semiconductor device of claim 1, wherein the calcium and boron dopants are present in the polysilicon in a ratio of about 1:1.

4. The semiconductor device of claim 1, wherein the calcium is substantially uniformly distributed throughout the polysilicon gate electrode.

5. The semiconductor device of claim 1, wherein the calcium is substantially concentrated at or near the polysilicon gate electrode/gate dielectric interface.

6. The semiconductor device of claim 5, wherein the calcium is at least partially integrated in the polysilicon crystal structure.

7. The semiconductor device of claim 5, wherein the calcium is present in a thin atomic layer at the gate electrode/gate dielectric interface.

8. The semiconductor device of claim 6, wherein the calcium dopant dose is about 0.5e15/cm^2 to 2e15 /cm^2.

9. The semiconductor device of claim 1, wherein the device is a CMOS device.

10. The semiconductor device of claim 1, wherein the device is a PMOS device.

11. A method of making a semiconductor device having a P-channel MOS field-effect transistor, the method comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on the substrate; and

forming a calcium and boron doped polysilicon gate electrode layer on the gate dielectric.

12. The method of claim 11, further comprising:

patterning and etching the polysilicon and dielectric layers layer to form a gate electrode;

implanting the substrate with dopant to form source and drain regions.

13. The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of boron doped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with calcium such that the calcium is substantially concentrated at the polysilicon/dielectric interface.

14. The method of claim 13, wherein the polysilicon layer is deposited to its full thickness prior to calcium implantation.

15. The method of claim 13, wherein the polysilicon layer is about 1000 to 1500 Å thick.

16. The method of claim 13, wherein the calcium implantation is conducted at a dose of about $0.5e15/cm^2$ to $2e15/cm^2$.

17. The method of claim 13, wherein the polysilicon gate electrode layer formation comprises:

forming a first thin layer of polysilicon on the gate dielectric layer;

implanting the calcium into the first layer of polysilicon; and

forming a second layer of polysilicon over the calcium doped first layer.

18. The method of claim 17, wherein the first layer of polysilicon is about 100 – 200 Å thick.

19. The method of claim 18, wherein the second layer of polysilicon is 800 – 1400 Å thick.

20. The method of claim 18, wherein the calcium implantation is conducted at a dose of about 0.2e15/cm^2 to 1e15/cm^2 and an energy of about 1-5 keV.

21. The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of undoped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with boron and calcium.

22. The method of claim 21, wherein boron implantation precedes calcium implantation.

23. The method of claim 21, wherein calcium implantation precedes boron implantation.

24. The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of calcium doped polysilicon on the gate dielectric layer;

implanting the deposited polysilicon with boron.

25. The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a first thin layer of calcium doped polysilicon on the gate dielectric layer;

depositing a second thicker layer of polysilicon on the first layer;

implanting the deposited polysilicon layers with boron.

26. The method of claim 11, wherein the polysilicon gate electrode layer formation comprises:

depositing a layer of boron and calcium doped polysilicon on the gate dielectric layer.